WHAT IS CLAIMED IS:

1. A method comprising:

forming a gate structure on a semiconductor substrate;

forming a sidewall layer overlying the gate structure and the semiconductor substrate, wherein the sidewall layer comprises a first portion overlying a first sidewall of the gate structure;

forming a photoresist structure adjacent to the first portion; and

subjecting the photoresist structure to an ion beam, wherein the photoresist structure shields at least part of the first portion from the ion beam.

2. The method of claim 1, wherein the step of subjecting comprises orienting the first sidewall to have a non-orthogonal tilt angle between a path of the ion beam and a surface of the first sidewall.

3. The method of claim 2, wherein subjecting further comprises the non-orthogonal tilt angle having an angle of incidence formed by the path of the ion beam and the surface of the first sidewall ranging between 7 degrees and 45 degrees.

4. The method of claim 2, wherein subjecting further comprises selecting the non-orthogonal tilt angle based upon a thickness of the sidewall layer and a height of the gate structure.

5. The method of claim 4, wherein subjecting further comprises selecting the non-orthogonal tilt angle based upon a height of the photoresist structure.

6. The method of claim 1, wherein subjecting further comprises the ion beam delivering a dose ranging from between 10^{12} to 10^{15} cm^{-2}.

7. The method of claim 1, wherein subjecting further comprises the ion beam comprises a species of an element with an atomic number greater than 9.

8. The method of claim 7, wherein subjecting further comprises the ion beam comprises an element selected from the group consisting of silicon, germanium, and neon.

9. The method of claim 1, wherein subjecting further comprises the ion beam comprises a species of an element with an atomic number less than 9.

10. The method of claim 1, wherein forming a sidewall layer comprises the sidewall layer comprising a nitride.

11. The method of claim 1, wherein forming a sidewall layer comprises the sidewall layer comprising an oxide.

12. The method of claim 1, further comprising:

anisotropically etching a first portion of a sidewall layer to form a spacer on a first side, and

implanting a dopant to form a source extension area on the first side and a drain extension area on a second side, wherein the source extension area underlies the gate structure by an amount greater than the drain extension area.

13. A method of forming a semiconductor device comprising:

forming a first gate structure having a first side facing a first direction, and a second side facing a second direction, wherein the first side and the second side are parallel to each other, and the first direction is substantially opposite the second direction;

forming a sidewall layer overlying the first gate structure, wherein the sidewall layer comprises a first sidewall layer portion overlying the first side, and a second sidewall layer portion overlying the second side; and

subjecting the first sidewall layer portion to an ion dose while the second sidewall layer portion is not subjected to the ion dose.

14. The method of claim 12 comprising:

forming a second gate structure having a first side facing the first direction, and a second side facing the second direction;

forming the sidewall layer overlying the second gate structure, wherein the sidewall layer comprises a third sidewall layer portion overlying the first side of the second gate structure, and a fourth sidewall layer portion overlying the second side of the second gate structure; and

shielding the third sidewall layer portion from the ion dose when the first side of the first gate is subjected to the ion dose.

15. The method of claim 12, further comprising:

anisotropically etching a first portion of the first sidewall layer portion overlying the first side to form a spacer on the first side;

anisotropically etching a second portion of the second sidewall layer portion overlying the second side to form a spacer on the second side; and

implanting a dopant to form a source extension area adjoining the first side and a drain extension area adjoining the second side, wherein the source extension area underlies the gate structure by an amount greater than the drain extension area.

16. The method of claim 12, further comprising forming a photoresist structure adjacent to the first the first side;

17. The method of claim 12, further comprising forming a photoresist structure adjacent to the second side;

18. The method of claim 12, further comprising orienting a substantially horizontal surface of the gate structure to form a non-orthogonal angle of incidence between a path of an ion beam and the substantially horizontal surface of the gate structure.

19. The method of claim 17, wherein the non-orthogonal angle of incidence ranges between 7 degrees and 45 degrees.

20. The method of claim 17, wherein the non-orthogonal angle of incidence is based upon the thickness of the sidewall layer and a vertical dimension of a photoresist structure.

21. The method of claim 12, wherein the ion dose ranges from between 10^{12} to 10^{15} cm^{-2}.

22. The method of claim 12, further comprising etching the sidewall layer to form a spacer adjoining the first side having a first thickness and a spacer adjoining the second side having a second thickness.

23. A method of forming a semiconductor device comprising:

forming a first plurality of gate structures overlying a substrate, each of the first plurality of structures comprising a first side facing a first direction, and a second side facing a second direction, wherein the first direction and the second direction are approximately opposite directions;

forming a spacer layer overlying the plurality of gates;

adjusting a tilt between an ion beam path and the plurality of gate structures to comprise a directional component in the second direction;

subjecting the first side of a second plurality of gate structures to a first ion dose, wherein the second plurality of gate structures is a subset of the first plurality of gate structures that is less than the first plurality of gate structures.

24. The method of claim 22 further comprising:

subjecting the second side of a third plurality of gate structures to a second ion dose, wherein the third plurality of gate structures is a subset of the first

plurality of gate structures that is less than the first plurality of gate structures.

25. The method of claim 23 wherein the third plurality of gate structures is substantially mutually exclusive to the second plurality of gate structures, wherein substantially mutually exclusive indicates that the first plurality of gates has less than 50 percent of members in common with the second plurality of gates.

26. The method of claim 23 wherein the third plurality of gate structures is substantially mutually exclusive to the second plurality of gate structures, wherein substantially mutually exclusive indicates that the first plurality of gates has less than 10 percent of members in common with the second plurality of gates.

27. The method of claim 23 wherein the third plurality of gate structures is substantially mutually exclusive to the second plurality of gate structures, wherein substantially mutually exclusive indicates that the first plurality of gates has less than 1 percent of members in common with the second plurality of gates.

28. The method of claim 22, further comprising:

anisotropically etching a first portion of the spacer layer overlying the first side to form a spacer on the first side;

anisotropically etching a second portion of the spacer layer overlying the second side to form a spacer on the second side; and

implanting a dopant to form a source extension area adjoining the first side and a drain extension area adjoining the second side, wherein the source extension area underlies the gate structure by an amount greater than the drain extension area.

29. A method comprising:

forming a gate structure on a semiconductor substrate;

forming a sidewall layer overlying the gate structure and the semiconductor substrate, wherein the sidewall layer comprises a first portion overlying a first sidewall of the gate structure;

forming a photoresist structure adjacent to the first portion; and

subjecting the photoresist structure to an ion beam, wherein the photoresist structure shields at least part of the first portion from the ion beam.